3 predictions on the role of HLS for the 2020 Digital Platform

The latest ITRS tables (for 2011-2012 since the 2013 tables are not yet complete: http://www.itrs.net/reports.html) highlight three points that are important to anyone developing or using HLS/ESL solutions.

1. The responsibility for power reduction efforts will be shifted to higher abstractions.

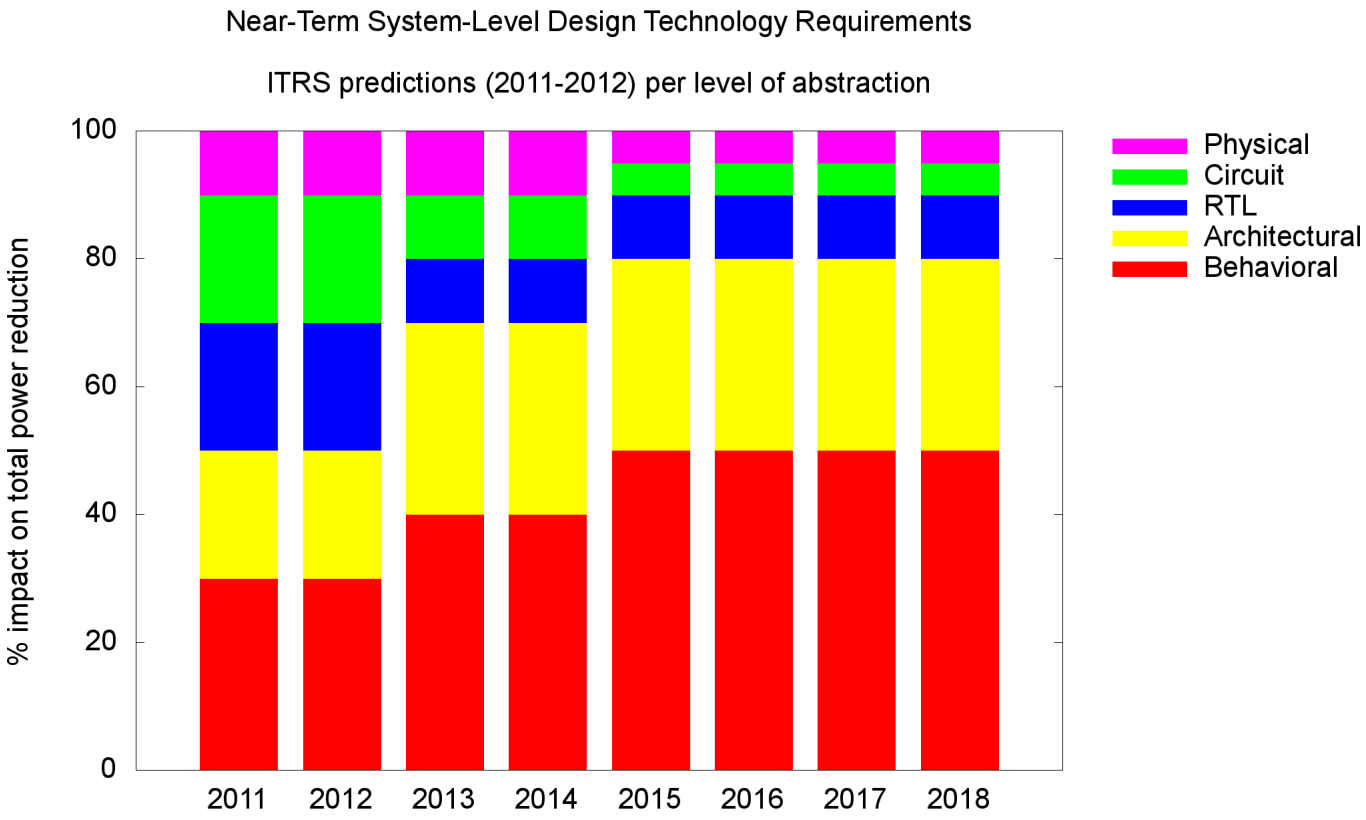

Figure 1: Power reduction effort for the 2020 Digital Platform.

Behavioral and architectural level requirements will rise from a 50% to an 80% contribution to overall system power reduction.

2. High-level synthesis estimates regarding speed, area, power and costs will be needed to be extremely accurate in the near future.

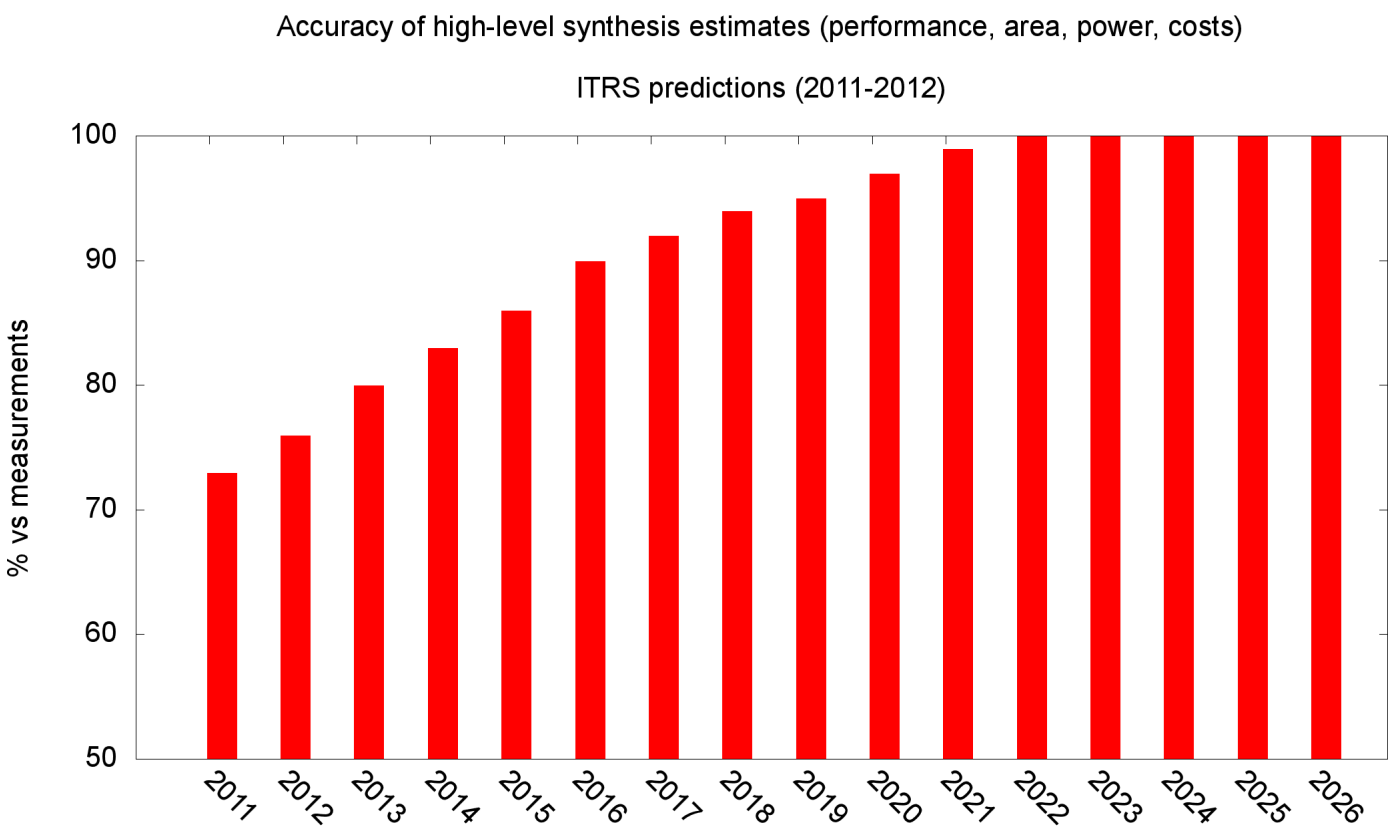

Figure 2: Expected high-level estimates accuracy for the 2020 Digital Platform.

The quality of estimations produced during the phase of architectural design space exploration is projected rise to an approximate 100% within less than 10 years! The tradeoff of better-vs-faster estimation will be even more evident.

3. The 2020 Digital Platform will be fully supported by development toolchains.

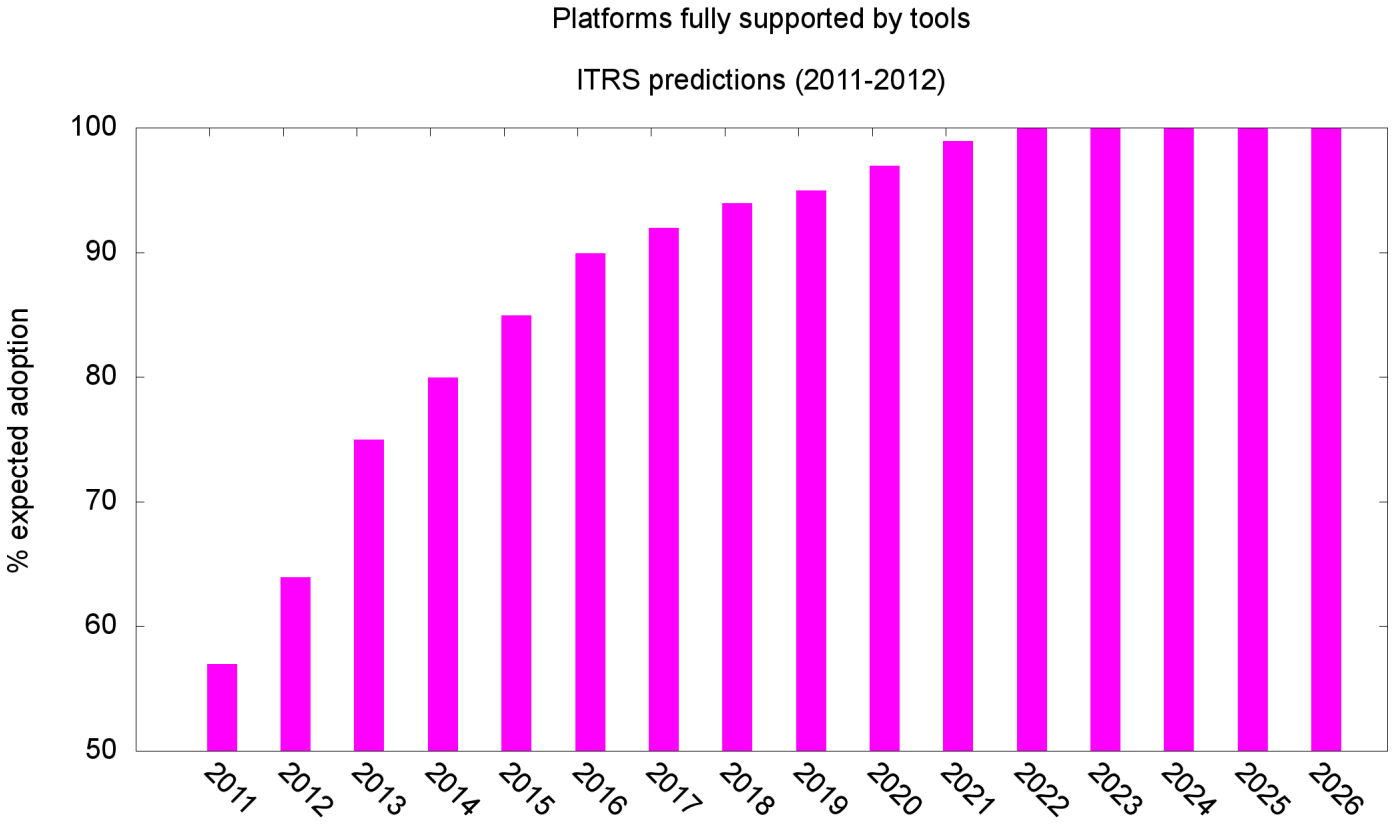

Figure 3: Expected levels of tool support for the 2020 Digital Platform.

This means that both programmable and configurable aspects of the platform (such as hardware accelerators) will be accessible via convenient layers of programmability. The current shift towards parallelism-aware languages including C/OpenMP, OpenCL, CUDA, AMP++, and OpenACC is clearly visible and a vibrant reality among programmers. The following figure indicates that within less than 10 years **ALL** computational platforms from the HPC realm to the autonomous, omnipresent, embedded systems will require full support by accessible tools.

What is your opinion?