perfeda

LOOPGEN
Hardware looping units

www.nkavvadias.com

Overview

The **LOOPGEN** IP collection provides fast hardware architectures for implementing nested loop structures. The collection comprises of a three different architectures (variants) adhering to a common I/O interface, namely **HWLU**, a mixed-level structural/RTL architecture, **IXGENB**, a behavioral-level and **IXGENR**, a high-performance, pure RTL description.

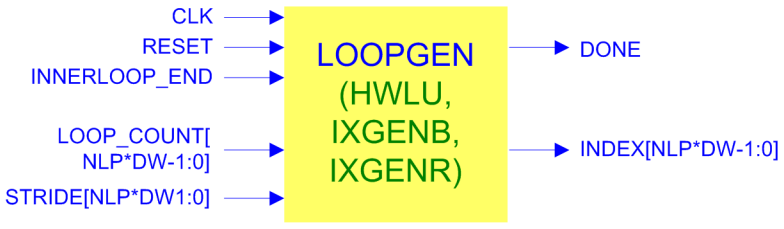
LOOPGEN can be used for data-intensive processing on multi-dimensional data. Each update of the iteration vector is evaluated with zero-cycle overhead.

Functional description

Each core uses a single external clock source, connected to signal CLK and can be reset with the active high signal RESET. INNERLOOP_END indicates that the innermost loop computations for the current iteration vector have completed. LOOP_COUNT and STRIDE provide the loop bound and step values for each loop. The loops are assumed to be enumerated from 1 to NLP, with the NLP-th being the innermost one. The iteration vector is represented by the INDEX output vector. DONE signifies the end of the computation for the entire loop structure.

The LOOPGEN IP can be viewed as implementing the following C-like looping structure in hardware:

```
for (i1 = 0; i1 < loop_count1; i1 += stride1) {
  for (i2 = 0; i2 < loop_count2; i2 += stride2) {...
      for (in = 0; in < loop_countn; in += striden) {
        // innermost loop computations}}}
```



FEATURES

- Three distinct architectures: Mixed-level structural/RTL, pure RTL and high-level/behavioral variants provided
- Support for any number of loops and datapath bitwidth (configured as generics)
- Compatible with the IEEE-1076 standard Uses the standard IEEE packages (numeric_std)
- Tested for large number of loops and large data bitwidths
- Simple block-level interface for bus-level integration to third-party designs

DELIVERABLES

- Documentation in ASCII text, PDF, HTML format
- Vendor-independent VHDL code for all architectures
- Configurable testbench
- Simulation (GHDL, Modelsim) and synthesis scripts (Xilinx XST/ISE)

Performance/QoR

IP architecture	Clock freq.	Area (LUTs/regs)	Time
HWLU	216	326 (0%)/ 81 (0%)	4.62 ms
IXGENR	243	242 (0%)/ 81 (0%)	4.11 ms
IXGENB	201	409 (0%)/ 81 (0%)	4.96 ms

Synthesis results on Xilinx XC6VLX75T for reference use.
Configured for NLP=5, DW=16.
Timing estimates for 1 million iterations.

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